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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,066	01/28/2004	Yoriharu Takai	04329.3226 9461	
7590 07/26/2006		EXAMINER		
Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.			ALPHONSE, FRITZ	
1300 I Street, N.W. Washington, DC 20005-3315			ART UNIT	PAPER NUMBER
			2133	

Please find below and/or attached an Office communication concerning this application or proceeding.

<u> </u>			
		Application No.	Applicant(s)
		10/765,066	TAKAI, YORIHARU
(Office Action Summary	Examiner	Art Unit
		Fritz Alphonse	2133
<i>TI</i> Period for R	he MAILING DATE of this communication app eply	ears on the cover sheet with the c	correspondence address
A SHORT WHICHE - Extensions after SIX (- If NO perior Failure to Any reply	TENED STATUTORY PERIOD FOR REPLY VER IS LONGER, FROM THE MAILING DAS of time may be available under the provisions of 37 CFR 1.13 (6) MONTHS from the mailing date of this communication. add for reply is specified above, the maximum statutory period we reply within the set or extended period for reply will, by statute, received by the Office later than three months after the mailing tent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION S6(a). In no event, however, may a reply be tin rill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).
Status	•		
2a) <u></u> Thi 3) <u></u> Sin	sponsive to communication(s) filed on <u>28 Ja</u> s action is FINAL . 2b)⊠ This ace this application is in condition for allowant sed in accordance with the practice under E	action is non-final. nce except for formal matters, pro	
Disposition (of Claims		
4a) 5)	tim(s) 1-12 is/are pending in the application. Of the above claim(s) is/are withdraw tim(s) is/are allowed. tim(s) 1-12 is/are rejected. tim(s) is/are objected to. tim(s) are subject to restriction and/or Papers specification is objected to by the Examiner drawing(s) filed on 28 January 2004 is/are:	r. r	I to by the Examiner.
App Rep	olicant may not request that any objection to the collacement drawing sheet(s) including the correction of the collacement drawing sheet(s) including the correction is objected to by the Example 1.	drawing(s) be held in abeyance. Section is required if the drawing(s) is ob	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).
Priority unde	er 35 U.S.C. § 119		
12)⊠ Ack a)⊠ A 1.∑ 2.[3.[nowledgment is made of a claim for foreign b) Some * c) None of: Certified copies of the priority documents Certified copies of the priority documents	s have been received. s have been received in Applicati ity documents have been receive (PCT Rule 17.2(a)).	ion No ed in this National Stage
2) Notice of 3) Informatic	References Cited (PTO-892) Draftsperson's Patent Drawing Review (PTO-948) on Disclosure Statement(s) (PTO-1449 or PTO/SB/08) (s)/Mail Date 1, 13.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal F 6) Other:	

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1, 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Weng (U.S. Pat. No. 5,428,630).

As to claim 1, Weng (figs. 3-4) shows a control circuit for a memory device, comprising: an inverter (358; fig. 4A) which inverts all bits of data read out from the memory device (col. 10, lines 1-6). Wend teaches a decoder which executes error correction and decoding for an output of the inverter (col. 2, lines 4-16).

As to claim 3, Weng discloses a control circuit, wherein the memory device comprises a nonvolatile semiconductor memory device (fig. 1; col. 3, lines 3-9).

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Weng in view of Fukushima (U.S. Pat. No. 6,981,205).

As to claim 2, Weng does not explicitly disclose a control circuit, wherein the decoder detects that there is no error for an inverted value of all bits of an initial value after data in the memory device is erased.

However, the limitation is obvious and well known in the art, as evidenced by Fukushima (col. 8, lines 26-36).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Weng's system with the data storage apparatus, as disclosed by Fukushima. Doing so would provide a method for improving the error correcting probability to generate correct read data (col. 2, lines 40-42).

5. Claims 4, 7-8 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weng in view of Crisp (U.S. Pat. No. 5,043,943).

As to claim 4, Weng (figs. 3-4) discloses a control circuit for a memory device, including: a first inverter (358; fig.4A) which inverts all bits of data to be written into the memory device (col. 10, lines 1-6); a decoder which executes error correction and decoding for an output of the inverter (col. 2, lines 4-16). Weng discloses an encoder which executes error correction and coding for an output of the first inverter (col. 1, lines 60 through col. 2 line 3).

Weng differs from claim 4 in that he does not explicitly disclose a second and third inverter which invert bits of data.

However, in the same field of endeavor, Crisp discloses a control circuit provided for controlling a memory device including a second and third inverter which invert bits of data (fig. 6; col. 5, lines 48 through col. 6 line 6).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Weng's system with the cache memory, as disclosed by Crisp. By doing so would the write data control signals enable the write amplifier to independently write a predetermined number of parity bits into the memory (col. 2, lines 60-63).

As to claim 8, the claim differs from claim 4 by the additional limitation "a buffer which holds data temporarily". However, the limitation is obvious and well known in the art, as evidenced by Crisp (figure 4). See the motivation for the same reason disclosed in claim 4 above.

As to claims 7 and 12, Weng discloses a control circuit, wherein the memory device comprises a nonvolatile semiconductor memory device (fig. 1; col. 3, lines 3-9).

As to claim 11, Weng does not explicitly disclose a memory controller, including a selector which selectively supplies an output of the buffer and an output of the encoder to the memory device. However, the limitation is clearly disclosed by Crisp (fig. 3; col. 4, lines 3-22). See the motivation for the same reason disclosed in claim 4 above.

6. Claims 5-6 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weng in view of Crisp as applied to claims 4 and 8 above, and further in view of Fukushima.

As to claims 5-6 and 9-10, Weng discloses a control circuit, wherein a coding method of the encoder is a method in which the decoder detects that there is no error for an inverted value of all bits of an initial value after data in the memory device is erased (fig. 1; col. 8, lines 49-66).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892

Any response to this action should be mailed to:

Application/Control Number: 10/765,066

Art Unit: 2133

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

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ALBERT DECADY

SUPERVISORY PATENT EXAMINE

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse, whose telephone number is (571) 272-3813. The examiner can normally be reached on M-F, 8:30-6:00, Alt. Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fritz Alphonse

Art Unit 2133

July 21, 2006